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GARLICK HARRISON & MARKISON
P.O. BOX 160727
AUSTIN, TX 78716-0727

EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS

AND INTERFERENCES

Application Number: 10/008,872

Filing Date: November 08, 2001

Appellant(s): LIN ET AL.

Kevin L. Smith #38620

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/17/2008 appealing from the Office action mailed 4/13/2007.

(1) Real Party in interest

A statement identifying by name the real party interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Pub 2002/0183013	Auckland et al	12-2002

US 5968143	Chisholm et al	10-1999
US 6434630	Micalizzi et al	08-2002
US Pub 2002/0009075	Fesas, Nestor A. Jr.	01-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,3,5-7,11-17,20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland et al (US Pub 2002/0183013), in view of Chisholm et al (US 5968143), and further in view of Micalizzi Jr, et al (US 6434630).

As for claim 1, Auckland discloses a wireless transceiver device, comprising: modulation circuitry for modulating and demodulating signals that are transmitted over the airwaves (Fig 1: #100); frequency conversion circuitry for up converting and down converting between radio frequency signals and baseband frequency signals (Fig 1: #100); digital-to-analog conversion

circuitry for converting from analog to digital and from digital to analog (Fig 1: #100) (The RF/IF section 104 includes a receive module 110, a transmit module 112 and a frequency synthesizer 114. The receive module 110 generally includes a low noise amplifier (LNA), frequency downconversion, filtering, demodulation, analog to analog to digital conversion, etc., as indicated in FIG. 1.The transmit module 112 generally includes a frequency upconversion, filter, digital to analog conversion and modulation as indicated in FIG. 1;Auckland's paragraph 4, lines 1-8); a radio controller (Fig 1: #100) (The radio 100 includes a digital or baseband section 102, a radio frequency-to-intermediate frequency (RF/IF) section 104 and a radio frequency (RF) section 106;Auckland's paragraph 2, lines 1-2); and baseband processing circuitry including a first in first out memory structure for storing addresses for accessing data block. Auckland discloses a digital signal processor (Fig: 6: #614) to further process the baseband signal into digital packets. Auckand's paragraph 3 discloses that the base band section includes processor and memory elements to store receiving data/commands, to process these data/commands (see Aukland's paragraph 90) and transmitting data/commands to Fig 6: #616 Tx module. Auckland does not disclose the claim's detail of associating data structures to store data/commands in the baseband section as recited in the claim. However, Chisholm discloses a method to transfer data and command blocks between two sides (Chisholm 's Fig 3: host side and memory side), including a FIFO for storing addresses for accessing data blocks (Chisholm 's Fig 3: #311 registers set (i.e corresponding to the claim's FIFO) for storing command block address of each of the command block from host 103, column 5 lines 25-41), a plurality of command blocks formed with a memory structure, the command blocks include address of data blocks stored within random access memory (Chisholm's column 5 lines 25-39

creating/allocating command address queue portion (corresponding to the claim's command blocks), each command address queue associating with a register in the register set), and a memory portion storing an indicator for indicating whether a command block of the plurality of command block is in use (Chisholm's column 5 lines 30-34, host stores a transfer start signal/bit into the host command address register that corresponding to the command address queue portion, the start signal thus indicates the queue portion is in used). It would have been obvious to one of ordinary skill in the art at the time of invention to include the data structures and method as suggested by Chisholm in Auckland's system, thereby command/data blocks can be transferred quickly in an automatic manner by DMA circuit, eliminating overhead, without any further intervening from local and host processing units (Chisholm's column 5 lines 50-57).

Aukland and Chrisholm do not expressly disclose the command block structure that comprises addresses for accessing data blocks. However, Micalizzi discloses a command block structure having pointers that point to address of associating data segment (Micalizzi's column 8 lines 13-21). It would have been obvious to one of ordinary skill in the art at the time of invention to include the command block structure as suggested by Micalizzi in Auckland's system, thereby separate memory segment that storing data can be easily linked to the a particular command block associating with a particular host's I/O request (Micalizzi's column 8 lines 13-21; Chisholm's column 5 lines 50-57).

As in claim 3, Chrisholm discloses wherein the FIFO memory structure includes pointers that defines address of command block (Chisholm's column 5 lines 23-26 discloses creating command block address and associating command block address to the register in register set);

As for claim 5, Auckland discloses wherein the modulation circuitry includes Gaussian Phase Shift Keying modulation and demodulation circuitry (The radio may support any type of carrier modulation such as frequency modulation (FM), gaussian phase shift keying (GPSK), gaussian mean shift keying (GMSK), quadrature amplitude modulation (QAM) or other scheme now know or later developed; Auckland's paragraph 147, lines 2-4).

As for claim 6, Auckland discloses wherein the frequency conversion circuitry converts directly between radio frequency and baseband (Auckland's paragraph 76, lines 10-12 discloses an ACU capable of tuning to operate at different frequencies; Frequency information comes from baseband processor (Fig 6, DSP #614); The ACU 606 receives frequency, timing, and possibly other control signals at an input 628 from the synthesizer 612, or from the controller 614 as indicated by the dashed line in the drawing figure).

As in claim 7, the claim rejected based on the same rationale as in claim 1. Micalizzi further discloses storing a data block in random access memory (Micalizzi's column 8 lines 40-42).

As in claim 11, Michalizzi discloses address for a data block is only stored in a command block that being stored obviously to an available queue entries (Michalizzi's column 40-45). Chisholm further teaches that the available queue entries can be easily determined by the transfer start signal/bit (see Chishholm's column 5 lines 30-34).

As in claim 12, Chisholm's column 5 lines 23-26 discloses evaluating the address of a command block address stored within a FIFO pointer (creating command block address and associating command block address to the register in register set);

As in claim 13, Micalizzi discloses examining the content of the command block specified by the pointer to determine a data block address (Micalizzi's Fig 3A command block structures can be easily examined to determine the data block address Fig 3A: 110).

As in claim 14-15, Micalizzi discloses evaluating at least a first memory location of the data block whose address is stored in the command block to determine a data block size; retrieving an amount of data corresponding to the data block size (Micalizzi's Fig 3: data segment length #112, #116, column 8 lines 42-46), the data can easily be retrieved and transmitting that data to a radio modem for transmission over wireless airwave (see Auckland's Fig 6: #616).

As in claim 16, Chisholm's column 5 lines 30-34 clearly suggests when the transferring completed, the start/signal bit will be cleared.

As in claim 17, the claim rejected based on the same rationale as in claim 1.

As in claim 20, Chishholm's column 5 lines 30-34 disclose the defined memory portions for storing the command block indicators are each one bit in length.

As in claim 22, Micalizzi's column 6 lines 1-15 clearly disclose the SCSI command format relates to data transferring to particular devices (LUNs).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Auckland et al (US Pub 2002/0183013), Chisholm et al (US 5968143), Micalizzi Jr, et al (US 6434630) as applied to claim 17, and in view of Fesas, Jr (US 2002/0009075).

As in claim 21, Auckland, Chisholm, Micalizzi do not disclose the claim's specific length of the command block. However, Fesas discloses a command block data structure having length of 4 bytes (Fesas's paragraph 10). It would have been obvious to one of ordinary skill in the art

at the time of invention to include the command block structure having length of 4 bytes as suggested by Fesas in Auckland's system, thereby the command block can be fit into a word of memory (see Fesas's paragraph's 33 lines 1-6).

(10) Response to Argument

Appellant's arguments the rejections of claims 1, 3, 5-7, 11-17 and 20-22 are not persuasive.

A) Appellant argues, "the reconfigurable analog RF front end of Auckland does not recite memory structures for data transmission in a wireless environment", "Auckland does not recite data communication techniques, but instead reconfigurable analog front ends for radio". Examiner disagrees. Auckland's paragraph 90 states" The control 614 controls the operation of the RF portion 600. **In the illustrated embodiment, the controller 614 is embodied as a digital signal processor (DSP) and operates in conjunction with data and instructions stored in memory.** The memory may be integrated with the DSP or may be packaged separately. In other embodiments, the controller 614 may be embodied as a general purpose processor such as a microprocessor or microcontroller. **In still other embodiments, the functionality of the controller 614 may be partitioned among many devices and software routines of the radio including the RF portion 600**". (Emphasis added) Thus Auckland clearly teaches that processor 614, as DSP or any general purpose processor, can be used to process data and instruction of any software routines of the radio (i.e software defied radio, paragraph 85) , and not necessarily limiting to just the reconfiguration tasks for variety of air interface standards as Appellant assert. Examiner further notes that software routine executes in a processor inherently requires some sort of data structures.

Appellant further argues, "…Auckland does not recite an interaction of data memory and data transmission as set forth in Appellant's claimed invention". Examiner disagrees. As discussed above, Auckland clearly discloses components for data memory to interact with data transmission as shown in Fig 6, using software routine, DSP processor 614, rx module, Tx module and antenna.

Therefore Appellant's argument is not persuasive.

B) Appellant argues, "the command block transfer device of Chisholm relates to command control across components of a computer device, not a wireless transceiver device with command blocks including addresses of data blocks in a wireless environment". The argument is disturbing. Chisholm is relied for teaching command block/data structures with characteristics as claimed. The command/block data structures are used by a processor and software routine to execute the associating instructions and data, which are the same whether or not the environment is wire or wireless. In other words, Chisholm teaches using various circuitries, commonly known in the art, to convert wireless signal to digital signal (Auckland's Fig 6, antenna, RX module, Tx module) and readily to be processed by a processor and software routine Fig 6 614.

Therefore Appellant's argument is not persuasive.

Appellant further argues, "..The disparate Chisholm command blocks do not include "addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use". Examiner disagrees.

First, Chrisholm teaches the claimed limitation "a memory portion storing an indicator for indicating whether a command block of the plurality of command block is in use" (Chisholm's column 5 lines 30-34, host stores a transfer start signal/bit into the host command address register that corresponding to the command address queue portion, the start signal thus indicates the queue portion is in used).

Second, as stated in the rejection of claim 1, Examiner relies on Micalizzi for teaching of the limitation "command block includes addresses of data blocks.." (Micalizzi's discloses a command block data structure having pointer that point to address of associating data segment/data block, col. 8 lines 13-21). And it would have been obvious to one of ordinary skill in the art at the time of invention to include the command block structure as suggested by Micalizzi in Auckland's system modified by Chrisholm, and thereby separate memory segment/data block that stores data can be easily linked to a particular command block associating with a particular host's I/O request.

C) Appellant argues " …the host adaptor device of Micalizzi recites interrupt management techniques, not the use of command blocks with addresses of data blocks and indicators for command blocks in a wireless environment" , and "Micalizzi does not address ....indicator for command blocks" as set forth in Appellant's claimed invention.

In response, Appellant argument is not relevant because as discussed above, Examiner relies on Micalizzi for the teaching of a command block CDB having pointer 110,114 that point to address of associating data segment/data block as claimed. By using pointers which point to data segments, various data segments with different segment lengths can be easily stored anywhere in the memory and easily linked to a specific command block CDB (Micalizzi's

column 8 lines 13-21, “the data segment address(es) 110,114 is a starting address of a data segment stored in a memory 25 associated with a particular read or write I/O request", lines 40-46). And it would have been obvious to one of ordinary skill in the art at the time of invention to include the command block structure as suggested by Micalizzi in Auckland’s system modified by Chrisholm, and thereby separate memory segment/data block that stores data can be easily linked to a particular command block associating with a particular host’s I/O request.

Micalizzi’s additional teaching of interrupt is not relevant and in no way preclude the teaching of a command block structure includes addresses of data block as claimed.

D) Appellant’s argument regarding the rejection of claim 21 under U.S.C 103 is not persuasive.

Appellant argues, “Fesas recites address translation overhead reduction, not the use of command blocks with addresses of data blocks and indicators for command blocks in a wireless environment”.

In response, Examiner relies on Fesa for teaching of a command block with a specific block length of 4 bytes as claimed. Examiner does not rely on Fesa for teaching of claim’s other limitations simply because the other limitations are covered by Chisholm and/or Micalizzi. Fesa discloses a command block data structure having length of 4 bytes (Fesas’s paragraph 10). It would have been obvious to one of ordinary skill in the art at the time of invention to include the command block structure having length of 4 bytes as suggested by Fesas in Auckland’s system, thereby the command block can be fit into a word of memory (see Fesas’s paragraph’s 33 lines 1-6). Thus Fesa‘s teaching of the command block having length of 4 bytes can be

applied to any applications, in wire or wireless environment, because they all use commands and data structures stored in memory and to be processed by processor and software.

E) Appellant argues " prior art corollaries from disjointed art references were collected and then, by improperly using Appellant's claimed invention as the blueprint, improperly combined..". Examiner disagrees.

In response, Examiner relies on recited arts for teaching of various claim's limitations. The rational for combination of the recited prior arts are discussed above. In the arguments, Appellant cites additional features taught by the recited prior arts. However, Appellant fails to address the merits of the combination of recited prior arts as stated by Examiner in the rejections of the claims. Instead, Appellant merely attacks a recited prior art for features that already taught by another prior art or merely attacks by reciting additional features that are not relevant to the combinations of the recited prior arts.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/ Duc T. Doan/

Duc T. Doan

Examiner Art Unit 2188

Conferees:

/Hyung S Sough/
Supervisory Patent Examiner, Art Unit 2188
06/11/08

/Manorama Padmanabhan/
Quality Assurance Specialist, TC2100, WG 2180